

FIG. 1 - PRIOR ART

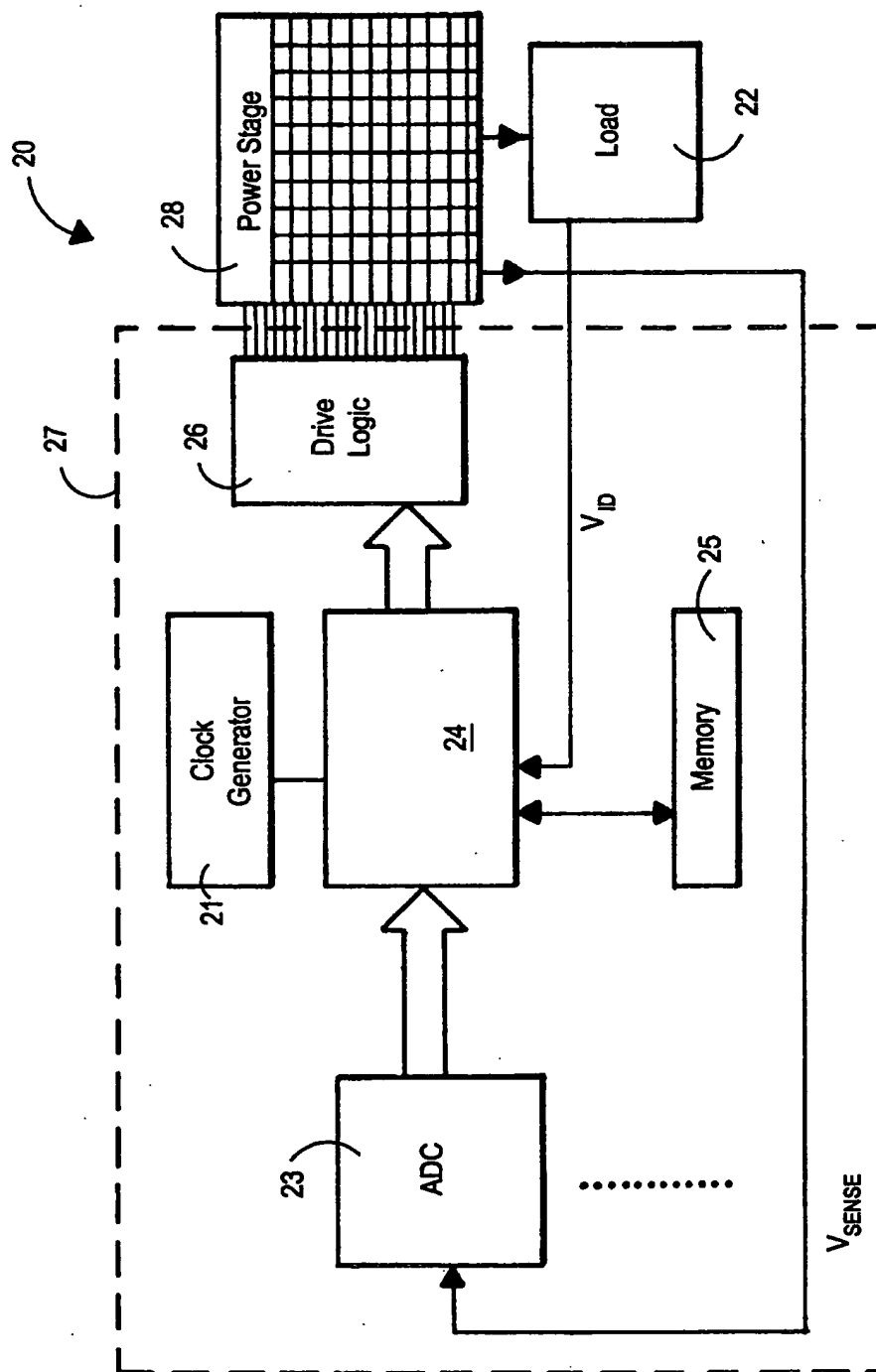


FIG. 2

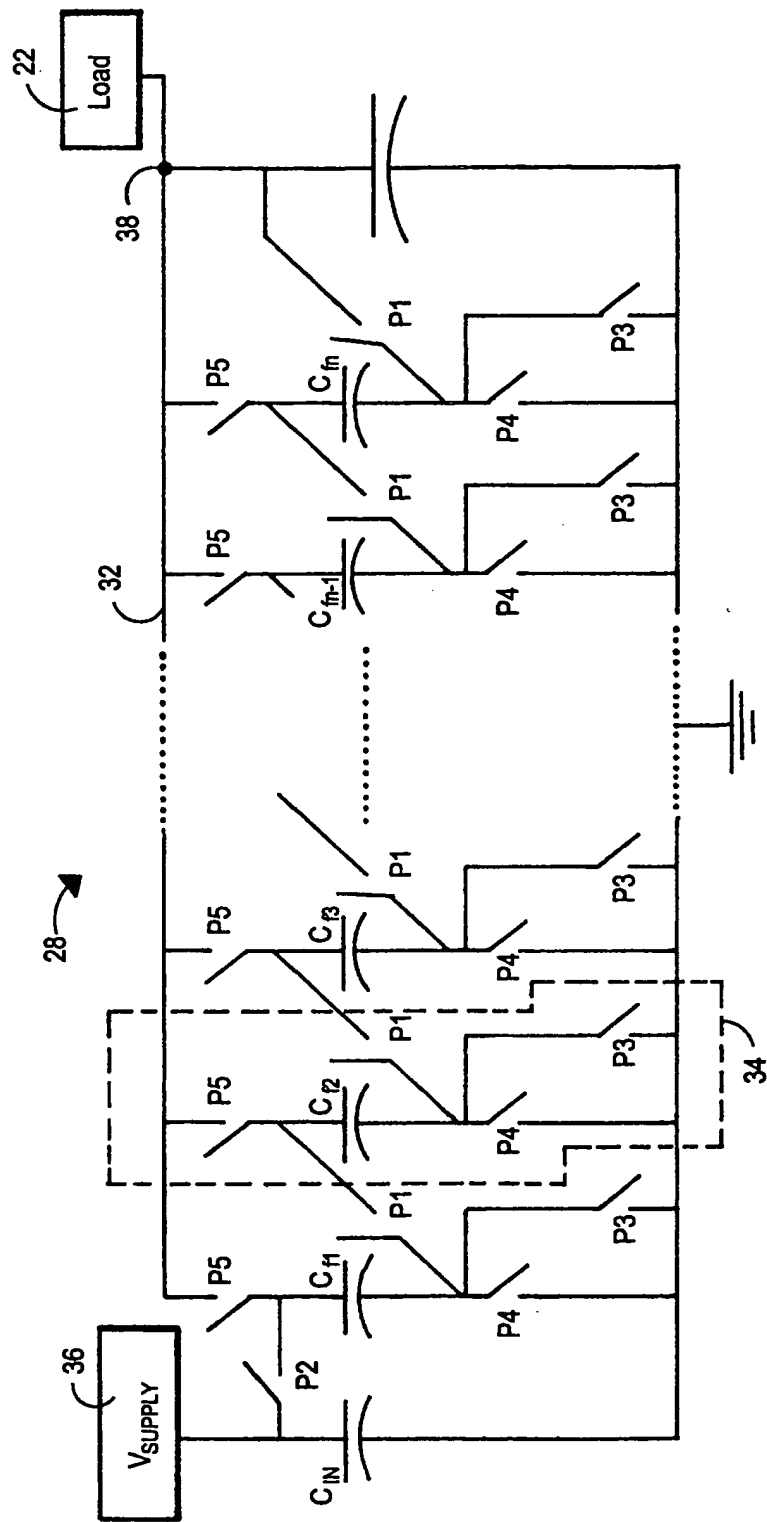


FIG. 3

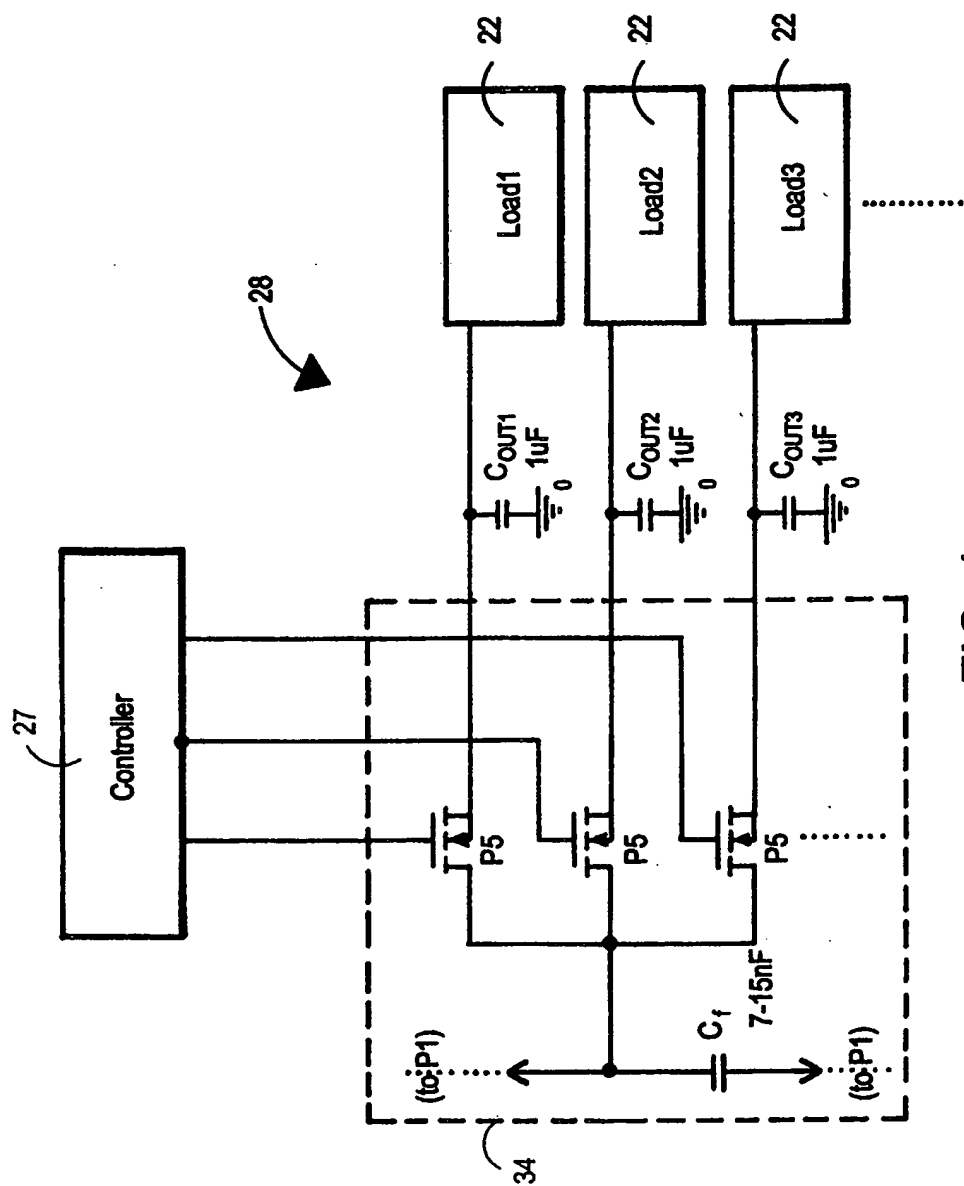


FIG. 4

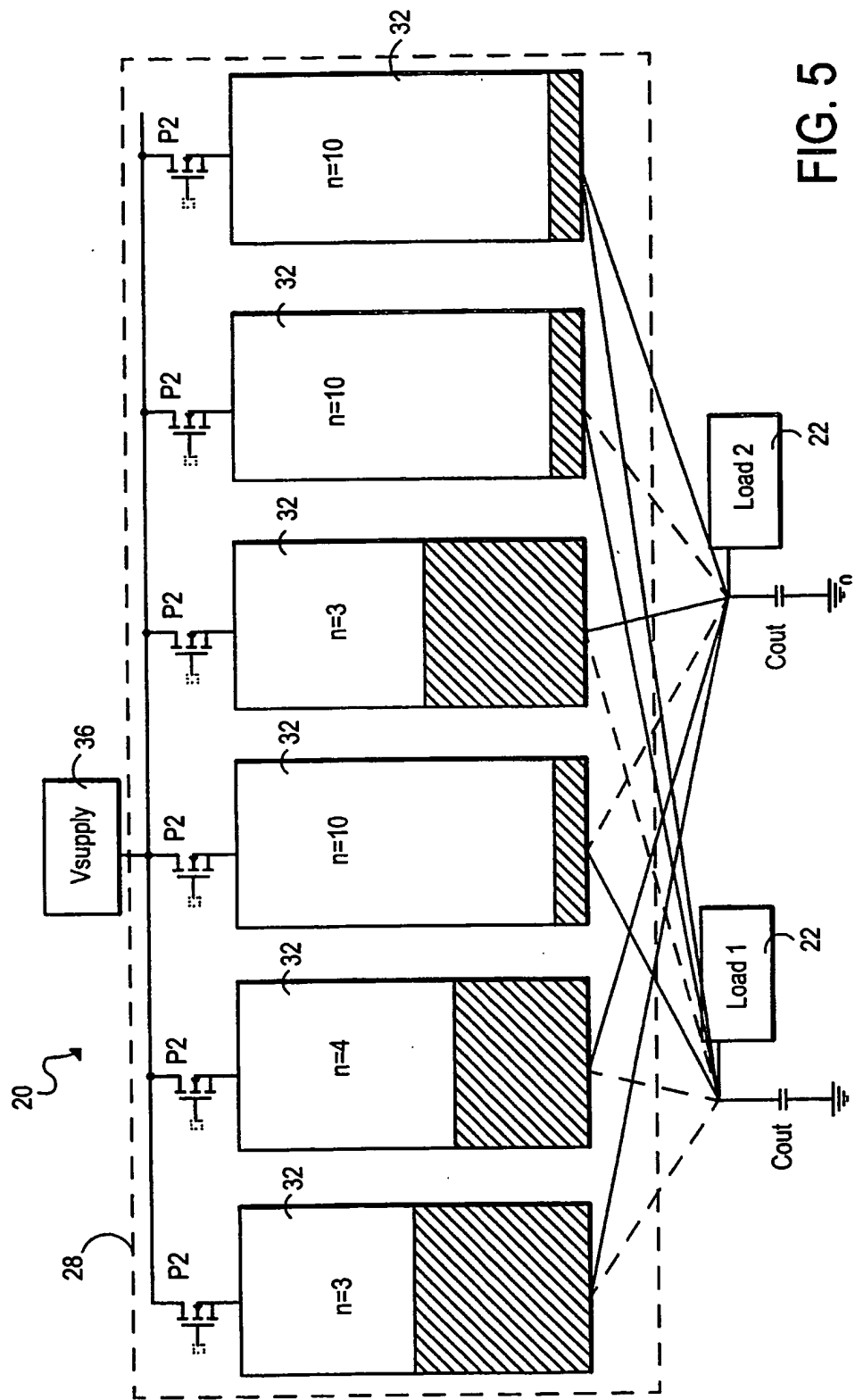


FIG. 5

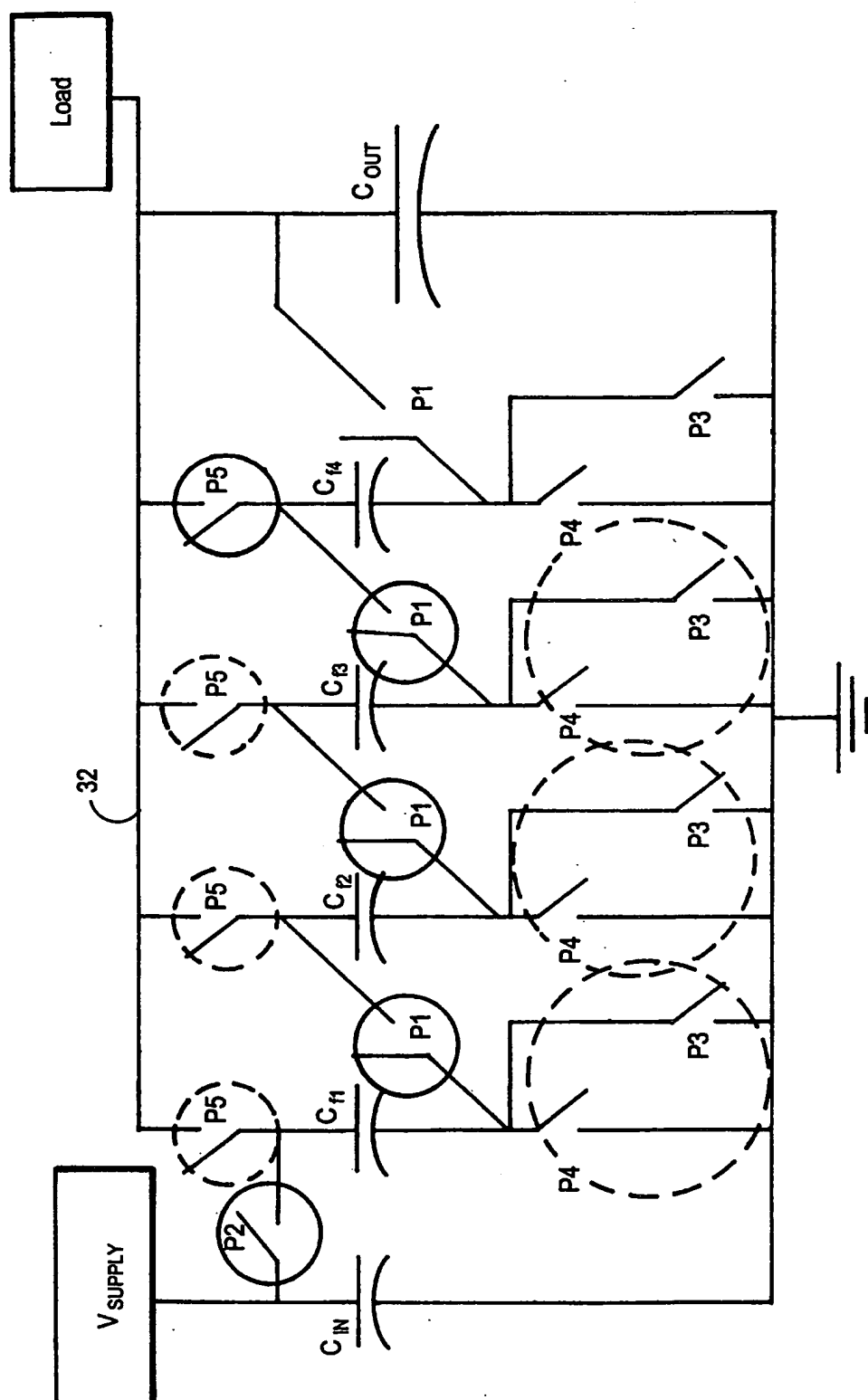


FIG. 6

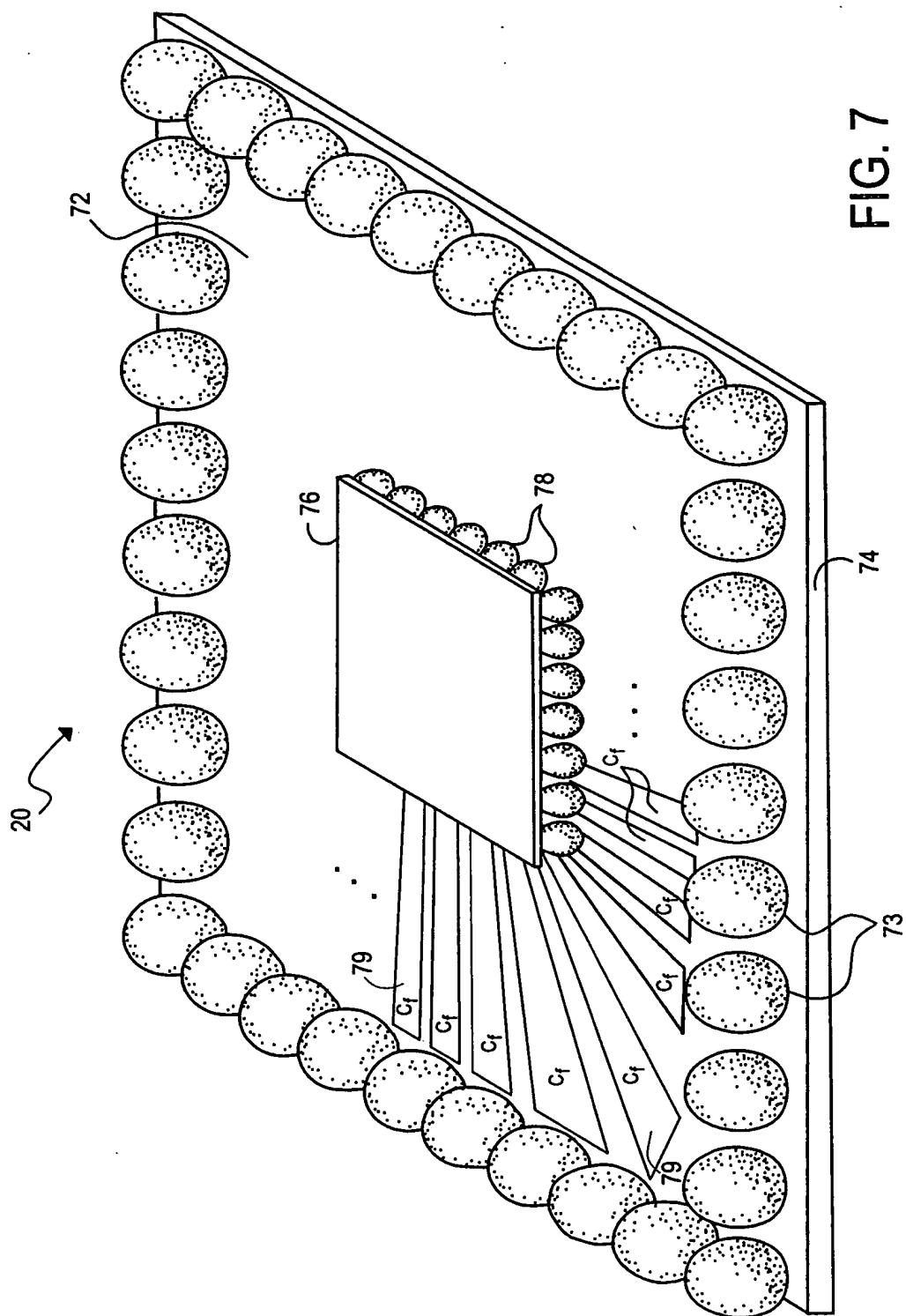
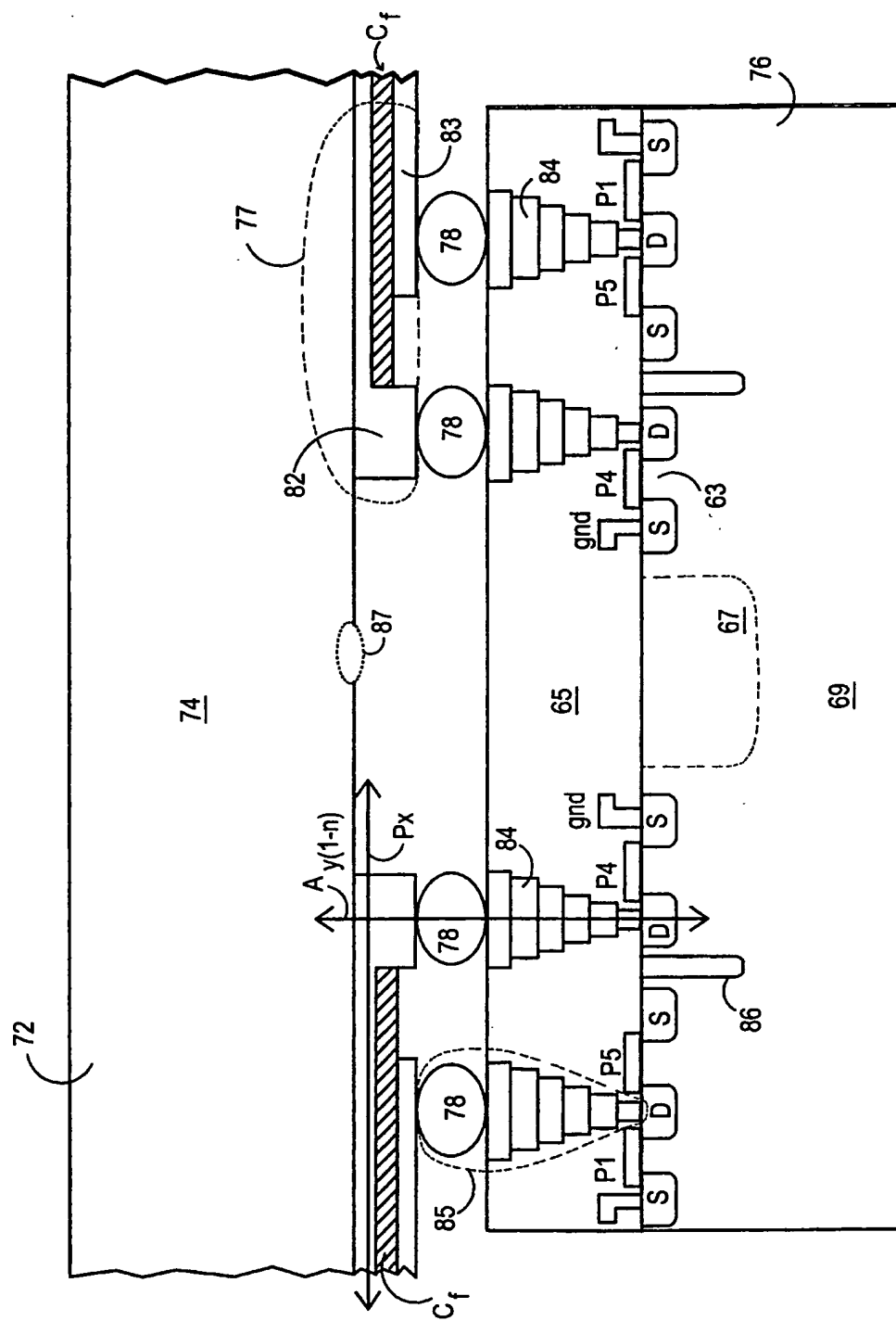


FIG. 7



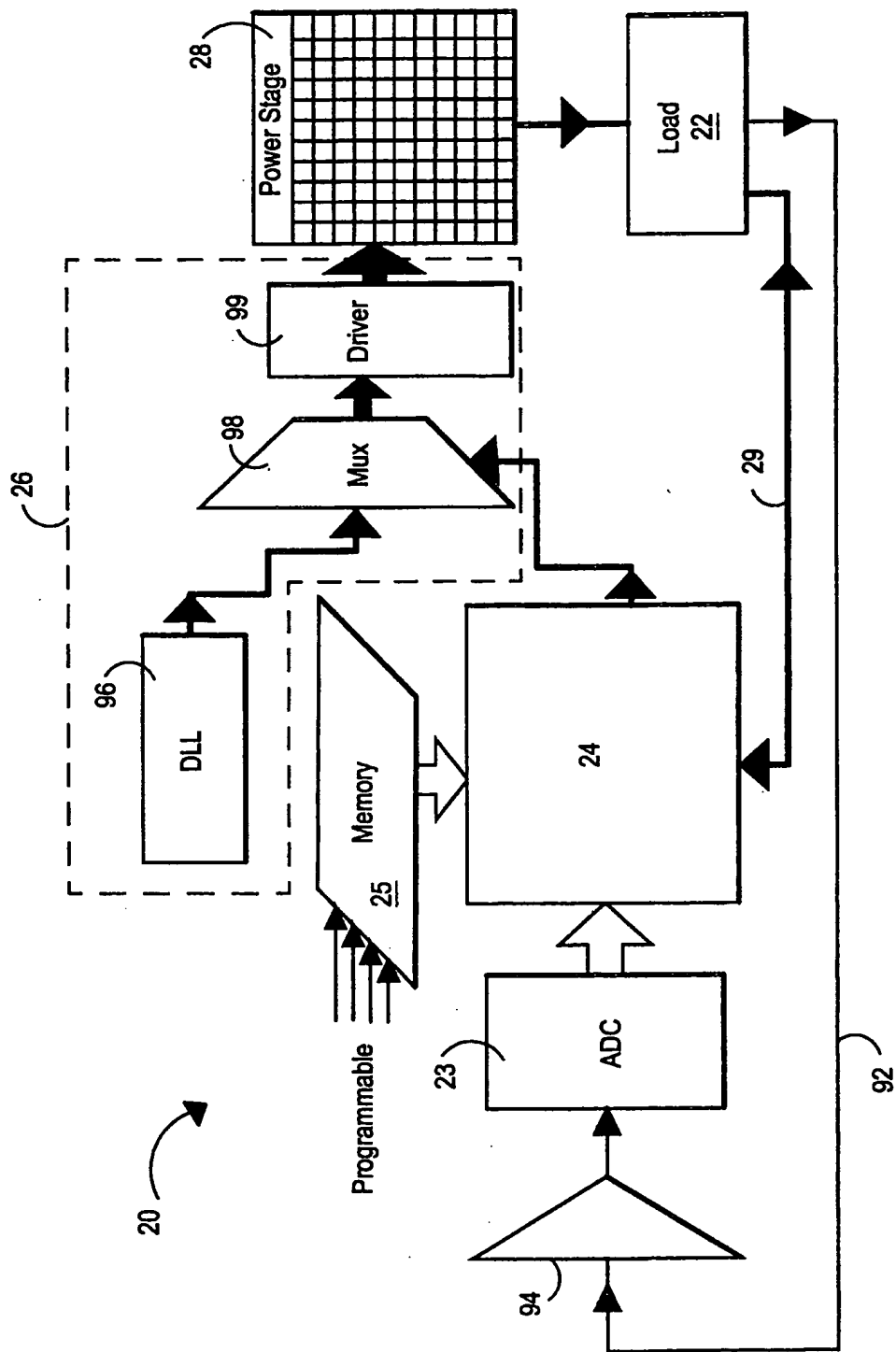
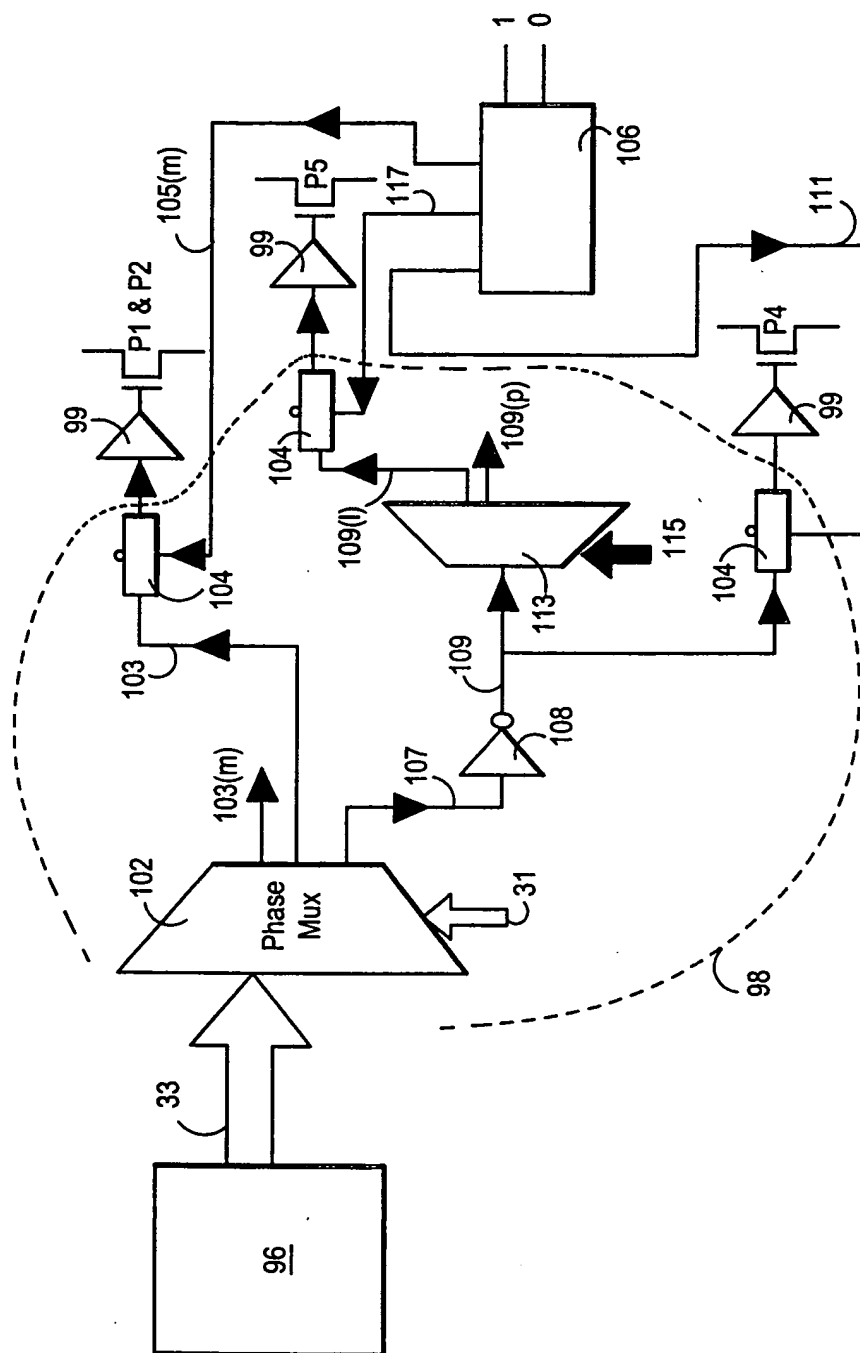


FIG. 9



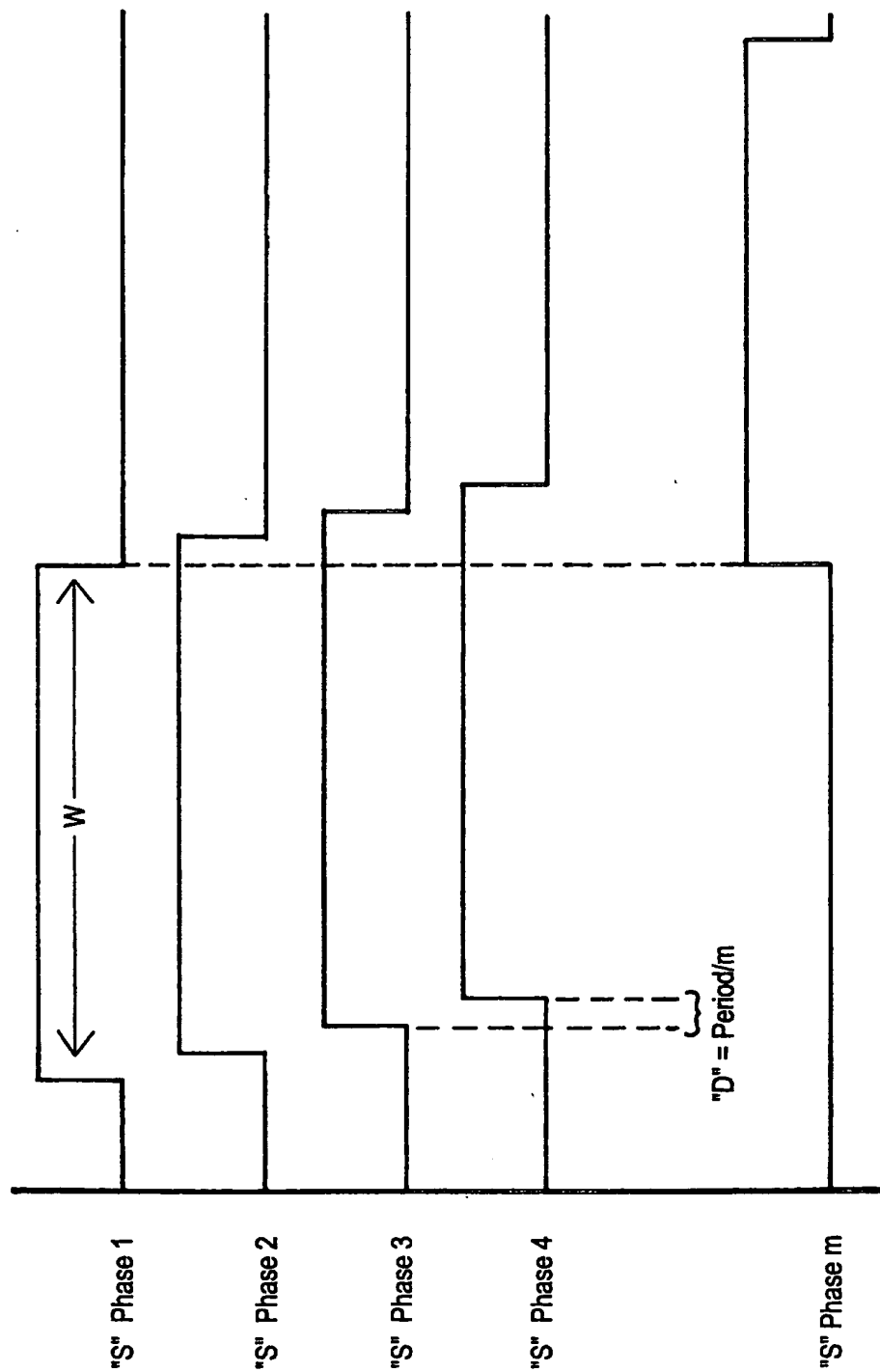


FIG. 11

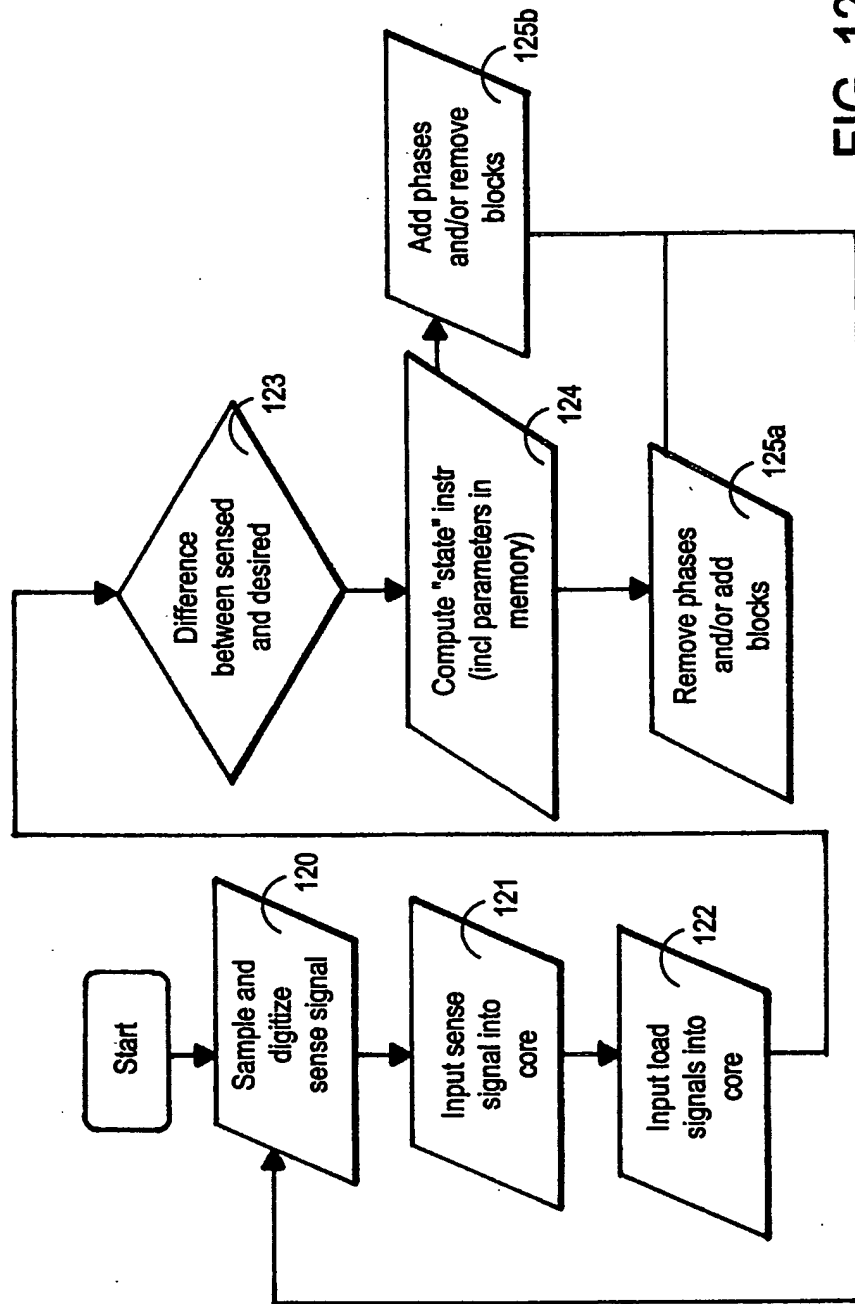


FIG. 12

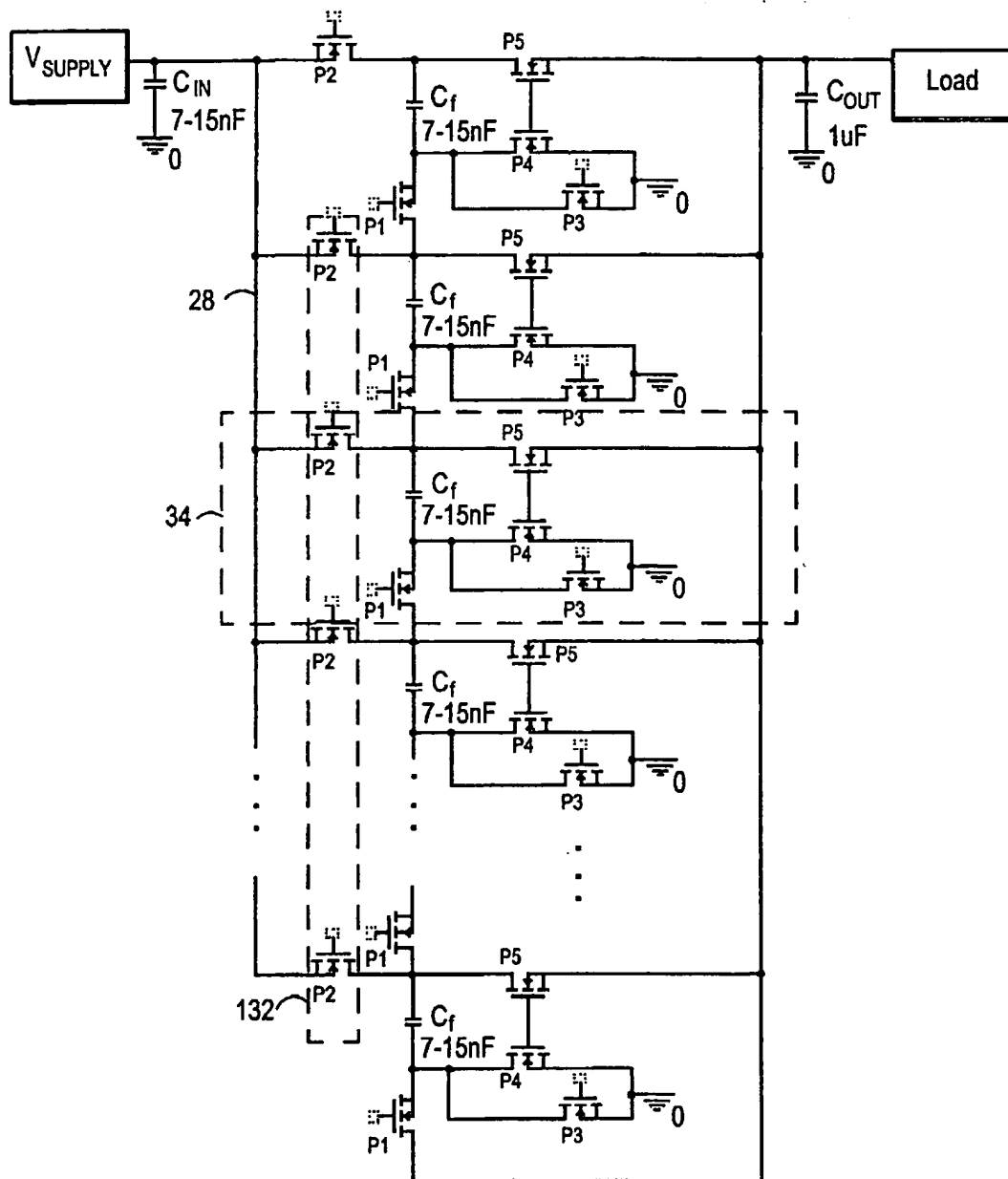


FIG. 13

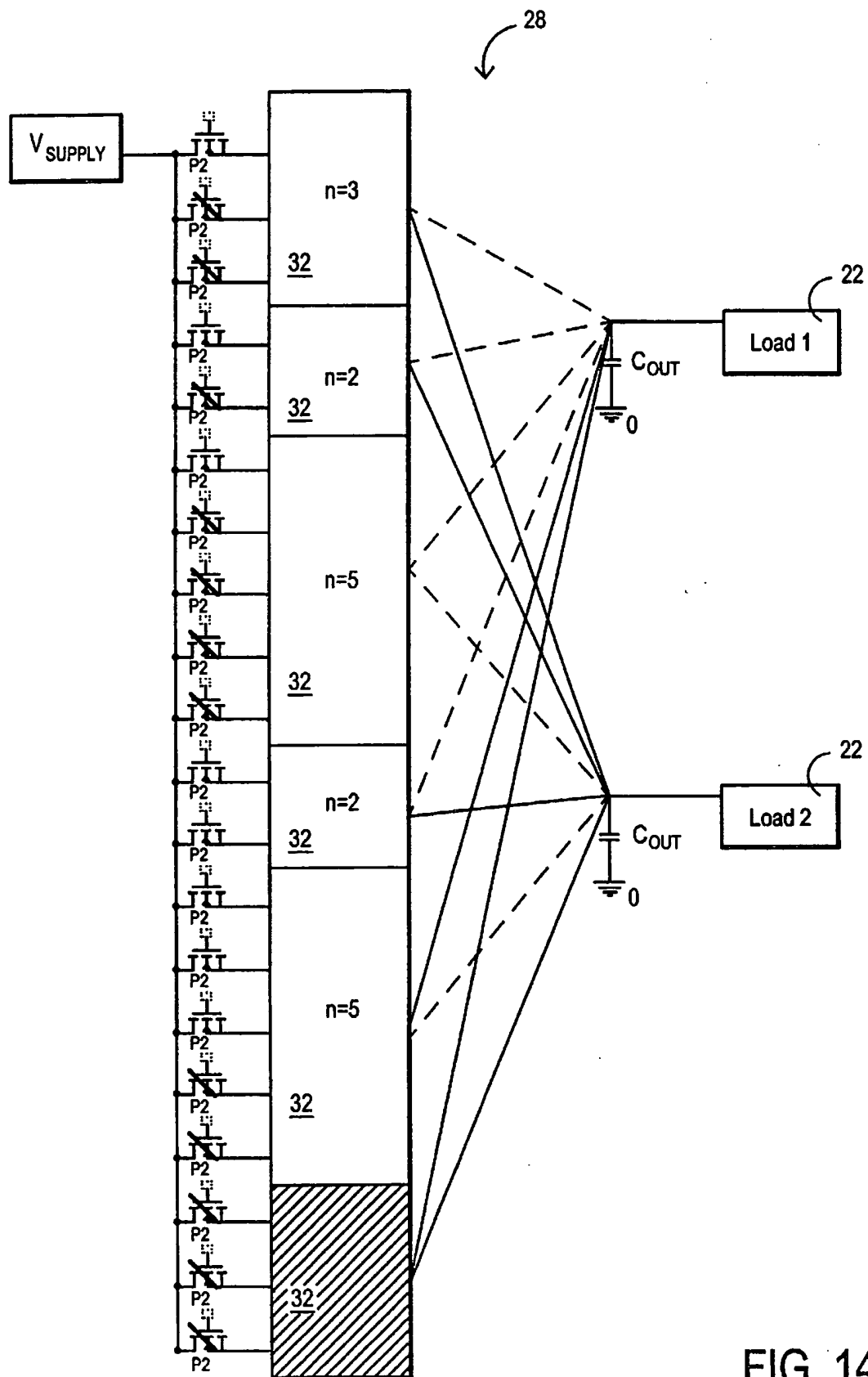


FIG. 14

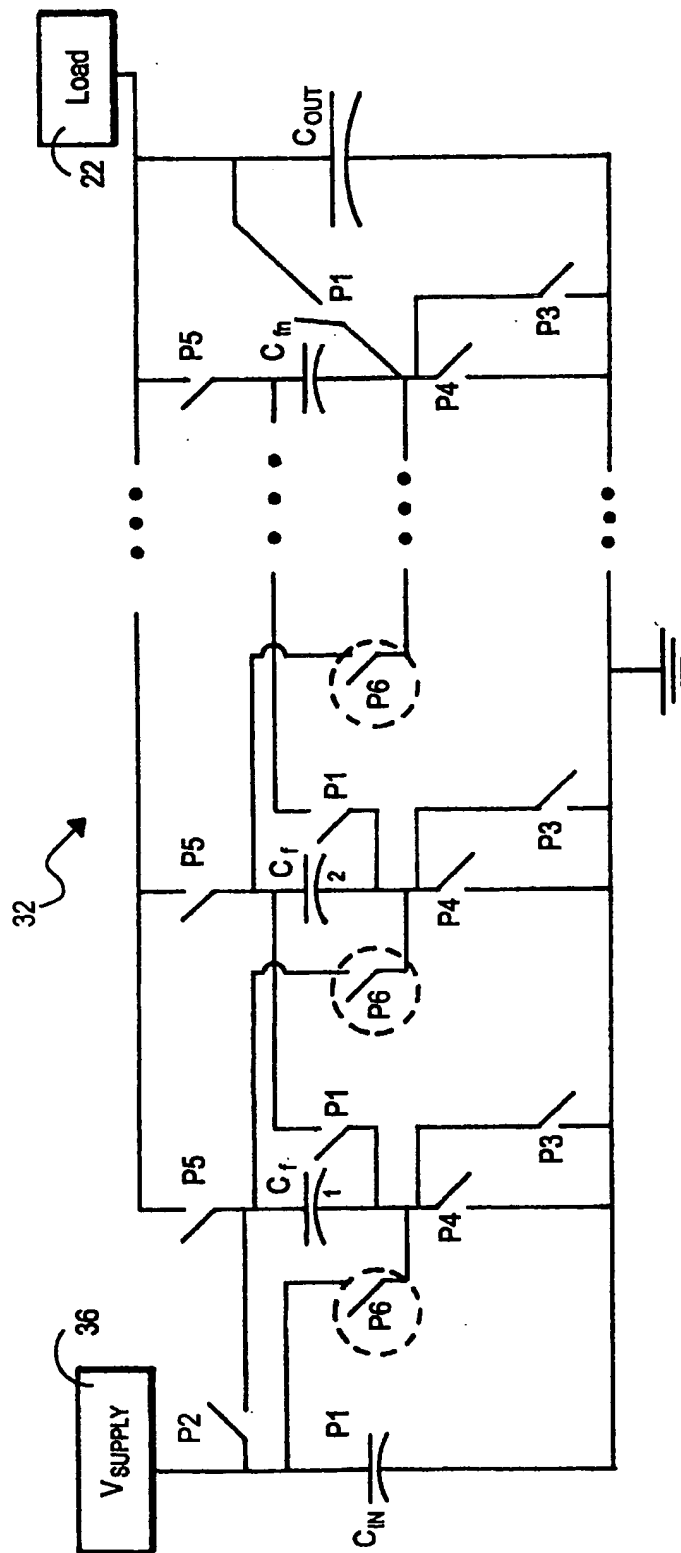


FIG. 15

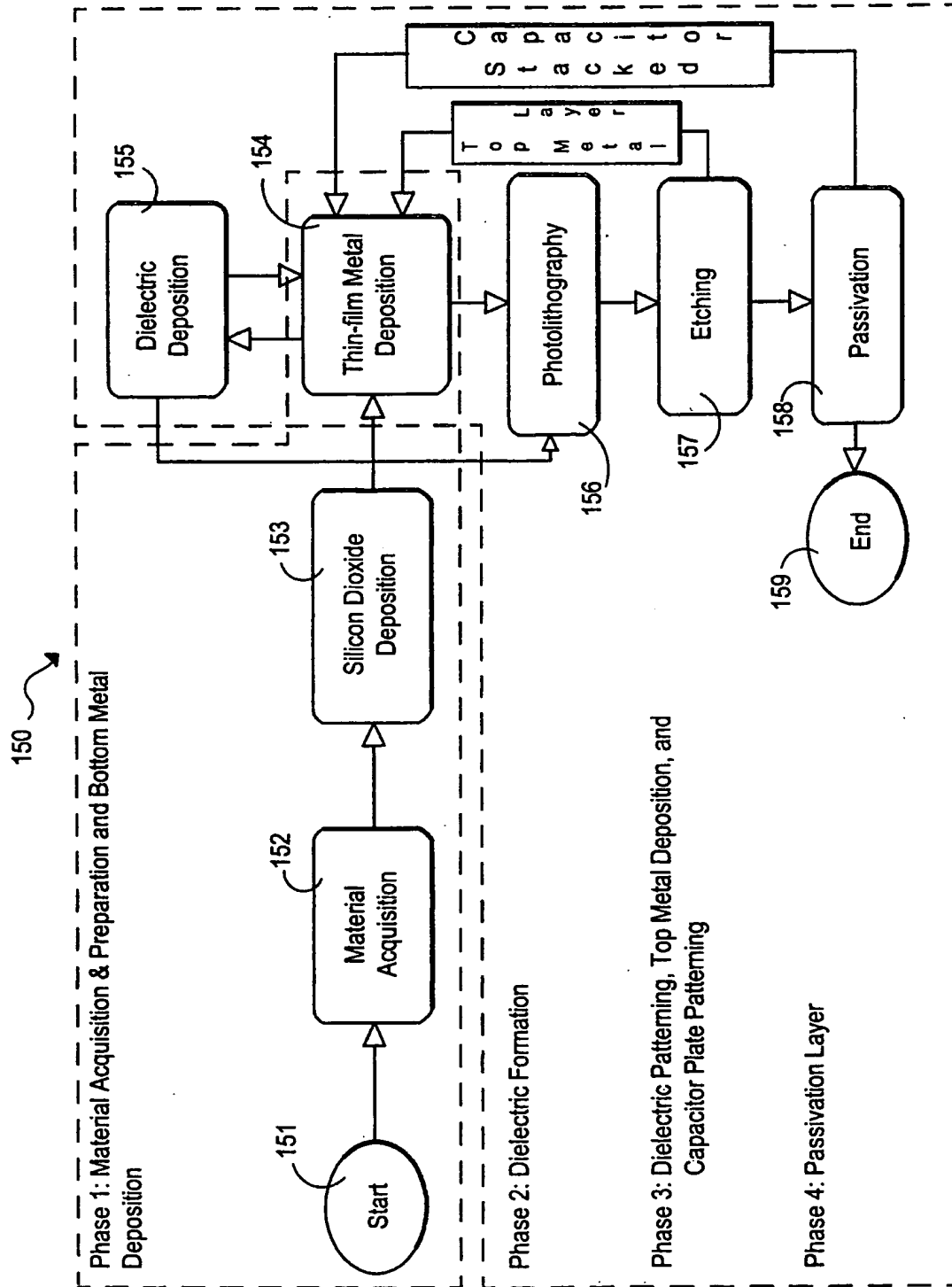


FIG. 16

PHASE	PROCESS STEPS	DESCRIPTION/NOTES
1	MATERIAL ACQUISITION & PREPARATION	
	Obtain Silicon Wafer	1 Standard 8" Silicon (6" for prototype)
	Deposit SiO ₂	2 0.5-1.0 μ m (insulation and adhesion)
	BOTTOM METAL DEPOSITION	
	Deposit Titanium	1 200 - 500 Å
	Deposit Copper	2 2 microns
	Deposit Tantalum	3 2000 Å
2	DIELECTRIC FORMATION	
	Tantalum Oxide Deposition	1 Anodization
3	DIELECTRIC PATTERNING	MASK 1
	Apply Resist	1 Typically 4 microns
	Exposure	2 Minimum feature size: 20 microns
	Develop	3
	Etch Tantalum Oxide	4 Typically RIE
	Etch Tantalum	5 Typically RIE
	TOP METAL DEPOSITION	
	Deposit Titanium	1 200 - 500 Å
	Deposit Copper	2 2 microns
	TOP METAL PATTERNING	MASK 2
	Apply Resist	1 Typically 4 microns
	Exposure	2 Minimum feature size: 20 microns
	Develop	3
	Etch Copper	4 Wet or dry
	Etch Titanium	5 Wet or dry
	Strip Resist	6
4	PASSIVATION (OPTIONAL)	
	Apply BCB	1
	Exposure	2
	Develop	3
	Cure	4

FIG. 17

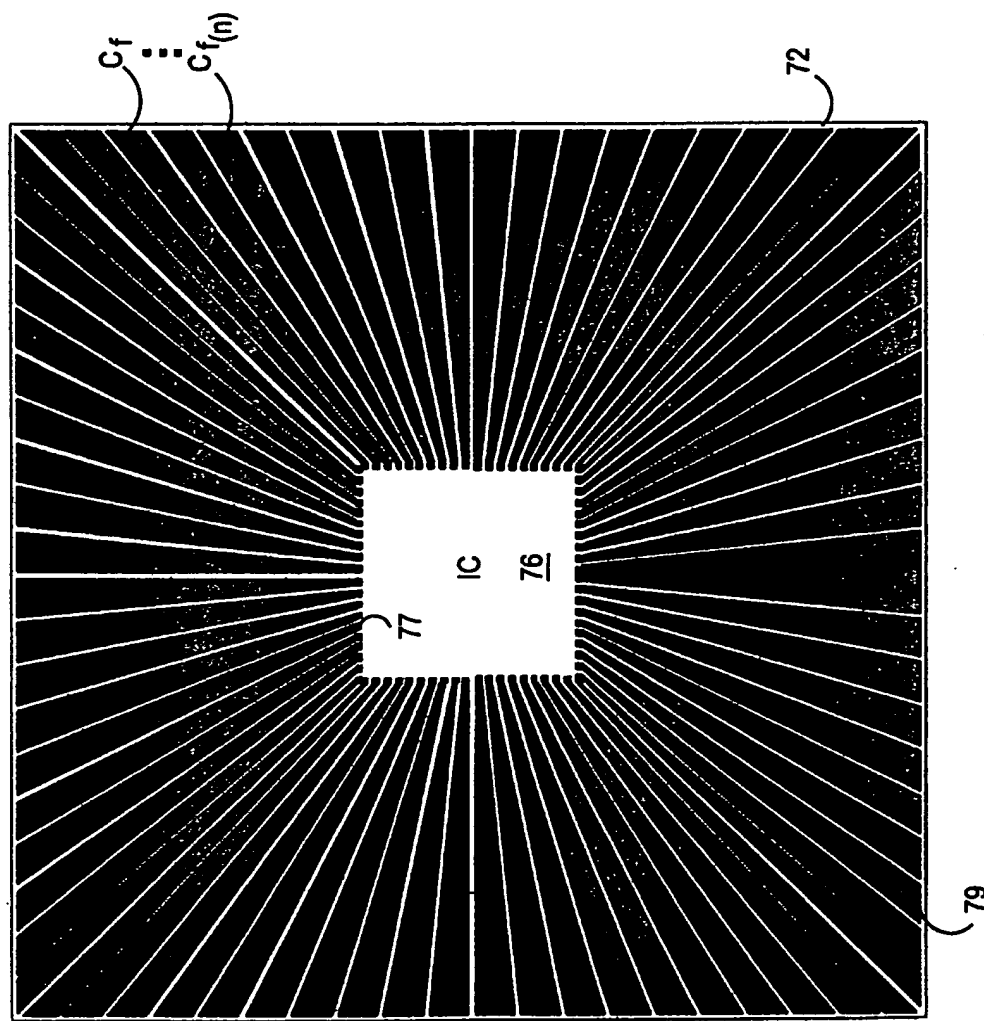


FIG. 18

BEST AVAILABLE COPY

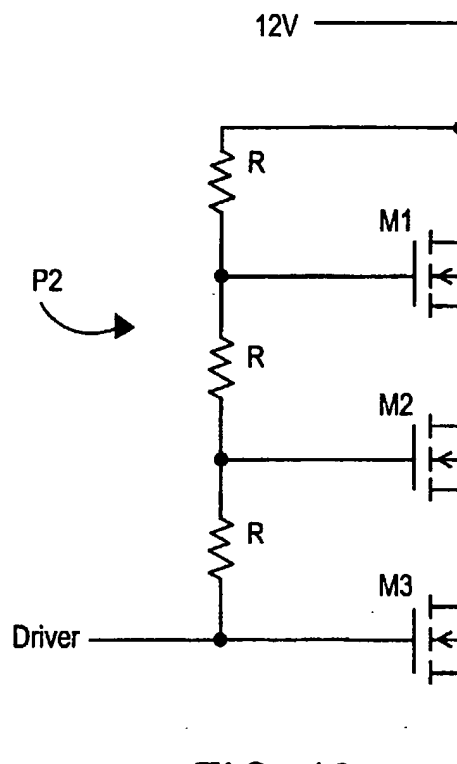


FIG. 19

Input Voltage	Gate Length (Process)	Qg(pC)	Fsw(MHz)
12	0.8 μm	>40	1-5
12	0.5 μm	27	10-20
5	0.5 μm	27	10-20
5	0.35 μm	20	20-30
3.3	0.35 μm	20	20-30
3.3	0.25 μm	10	50-60
3.3	0.18 μm	6	80-100

FIG. 20

Transient Up Response

1 A/ns transient. 6 ns [166 MHz] delay to model controller sampling and response

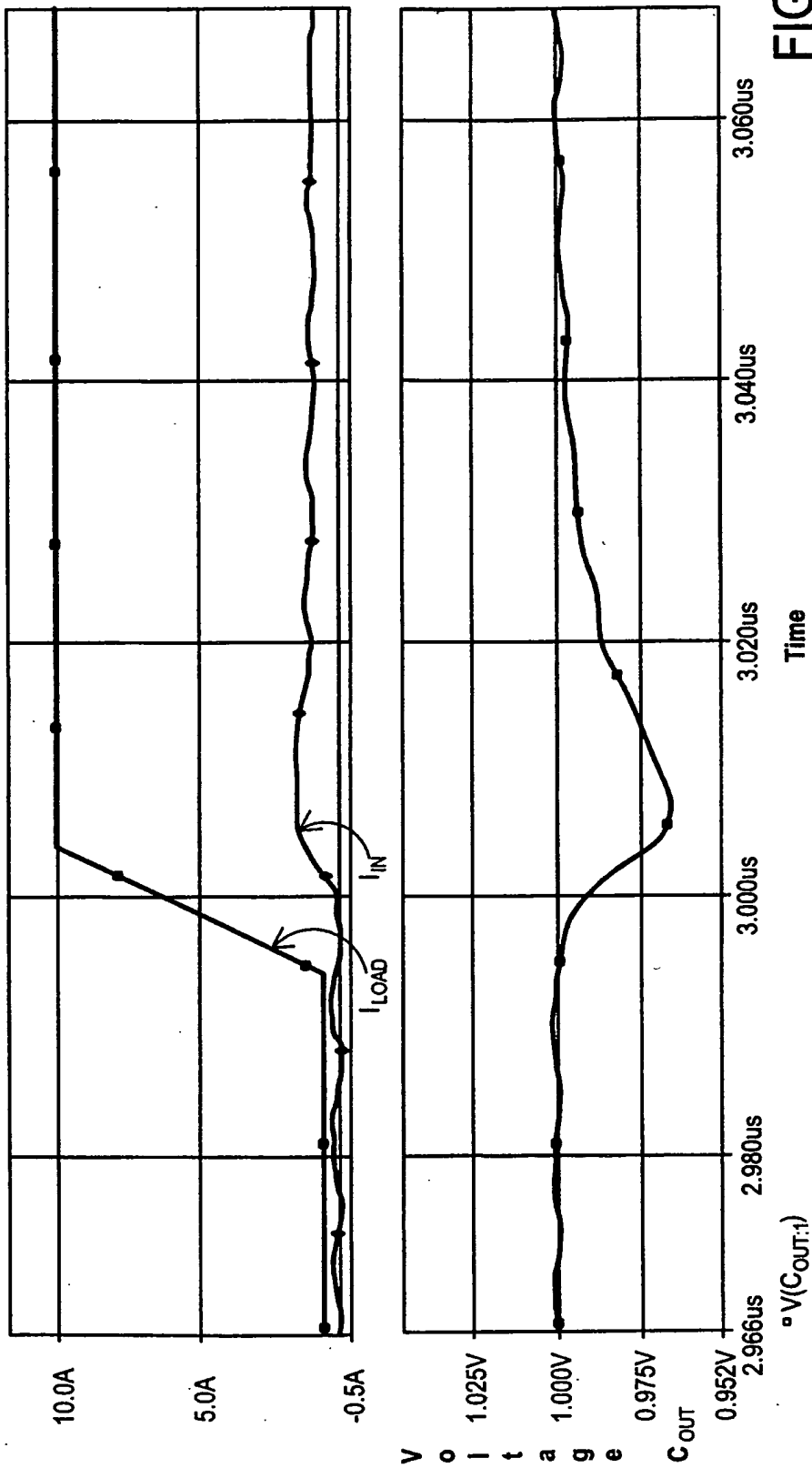


FIG. 21

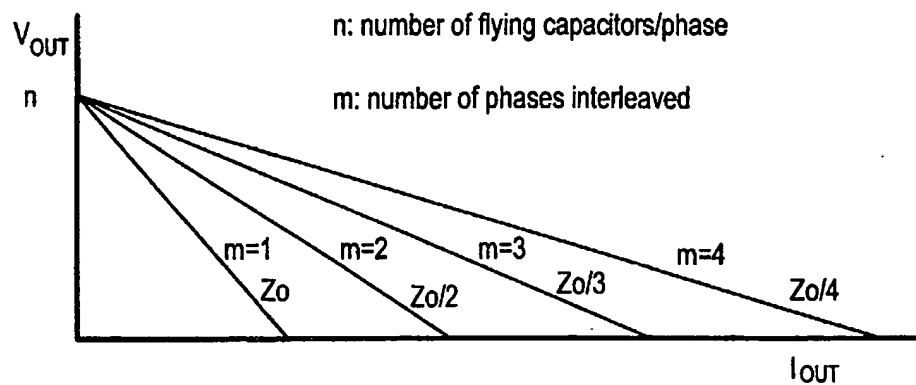


FIG. 22

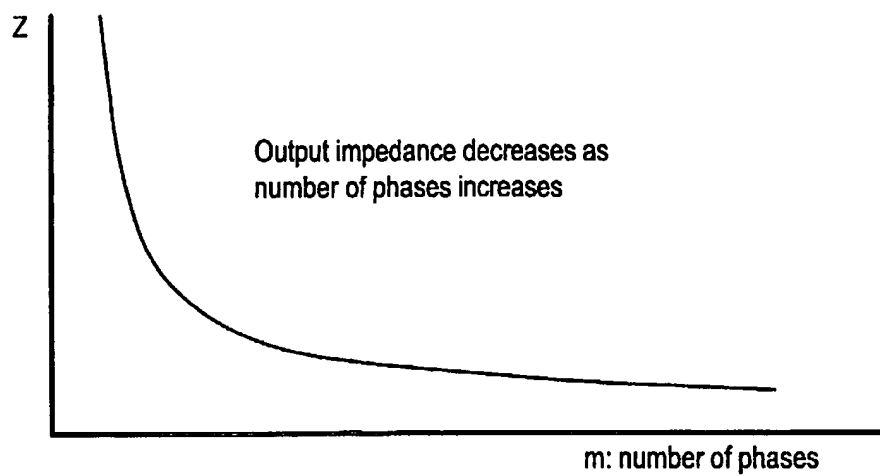


FIG. 23

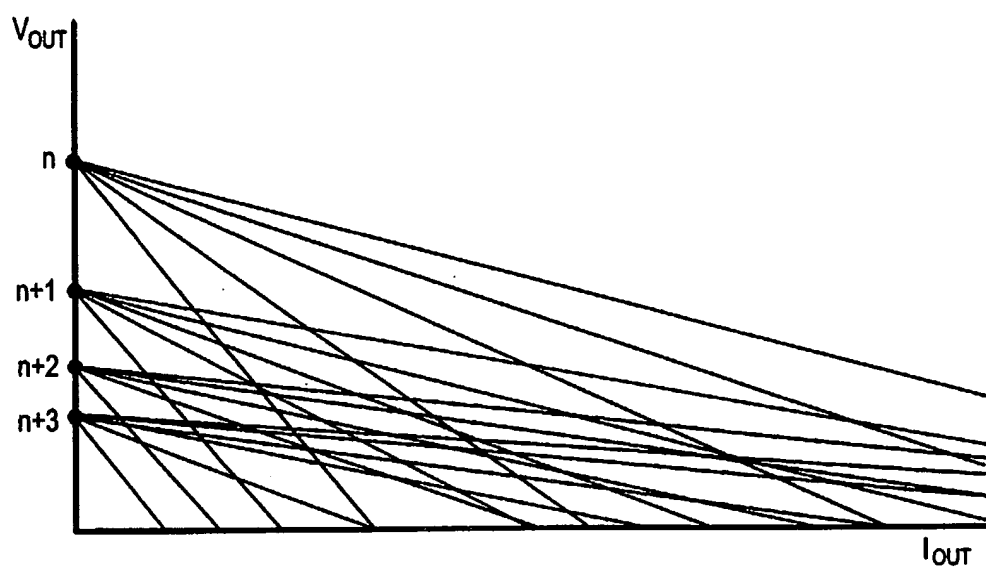


FIG. 24

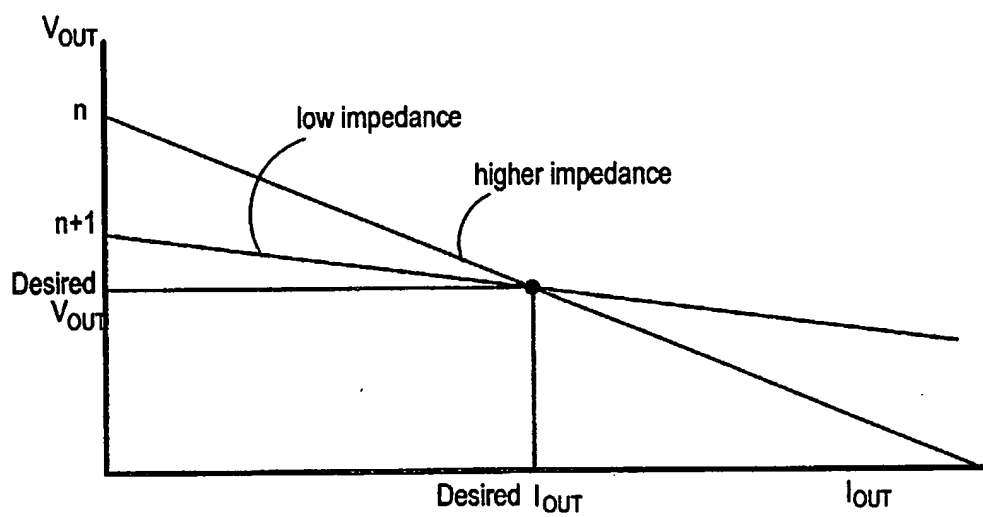


FIG. 25

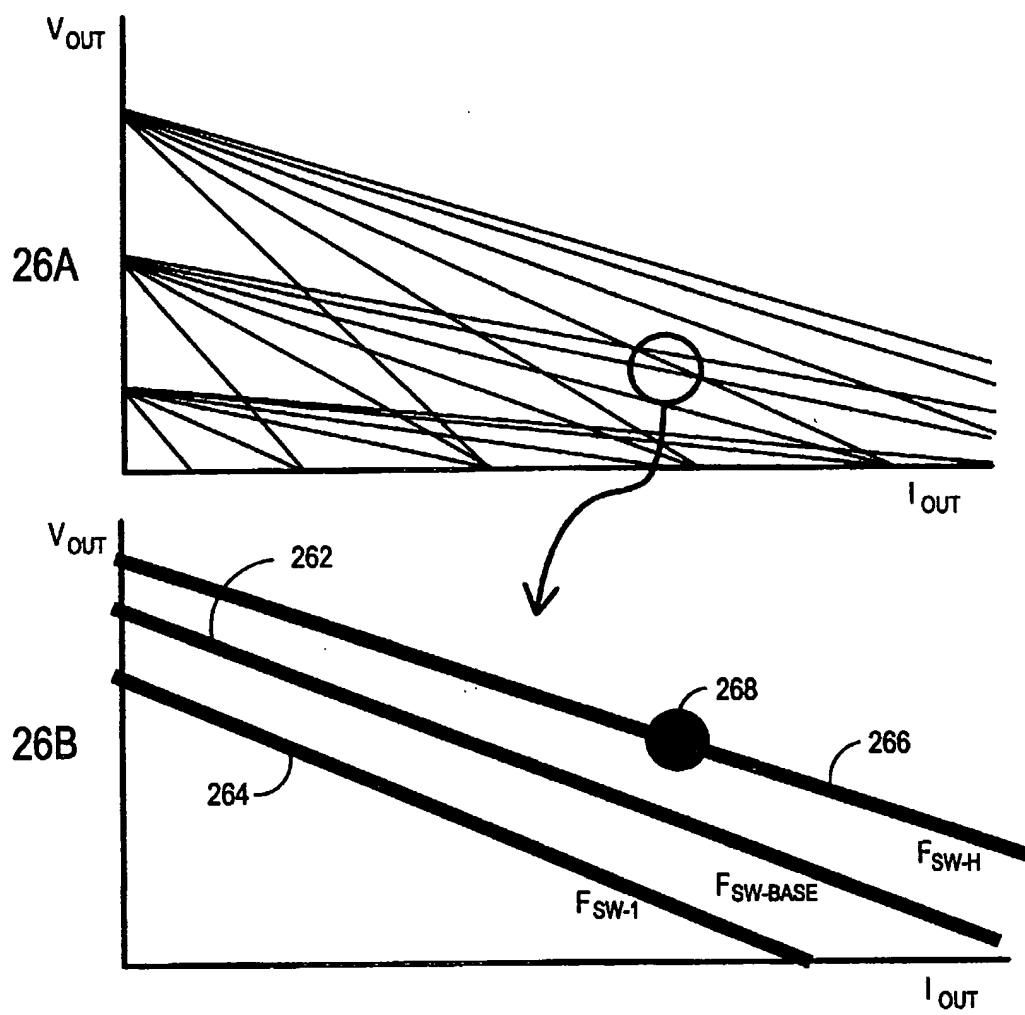


FIG. 26

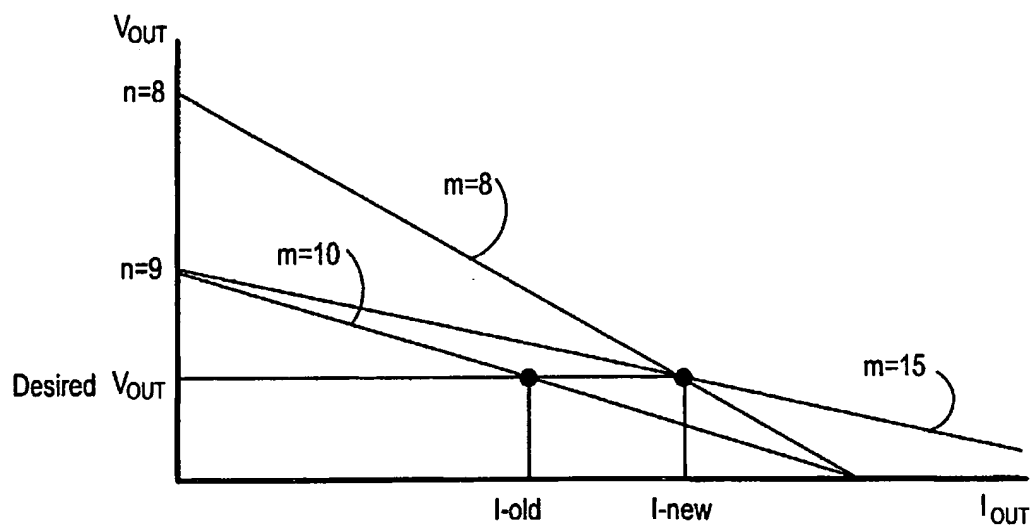


FIG. 27

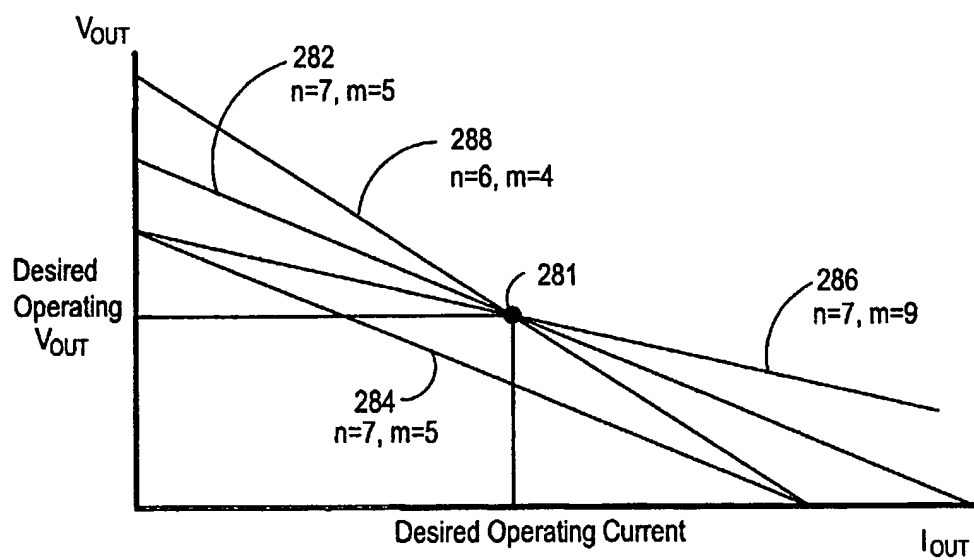


FIG. 28

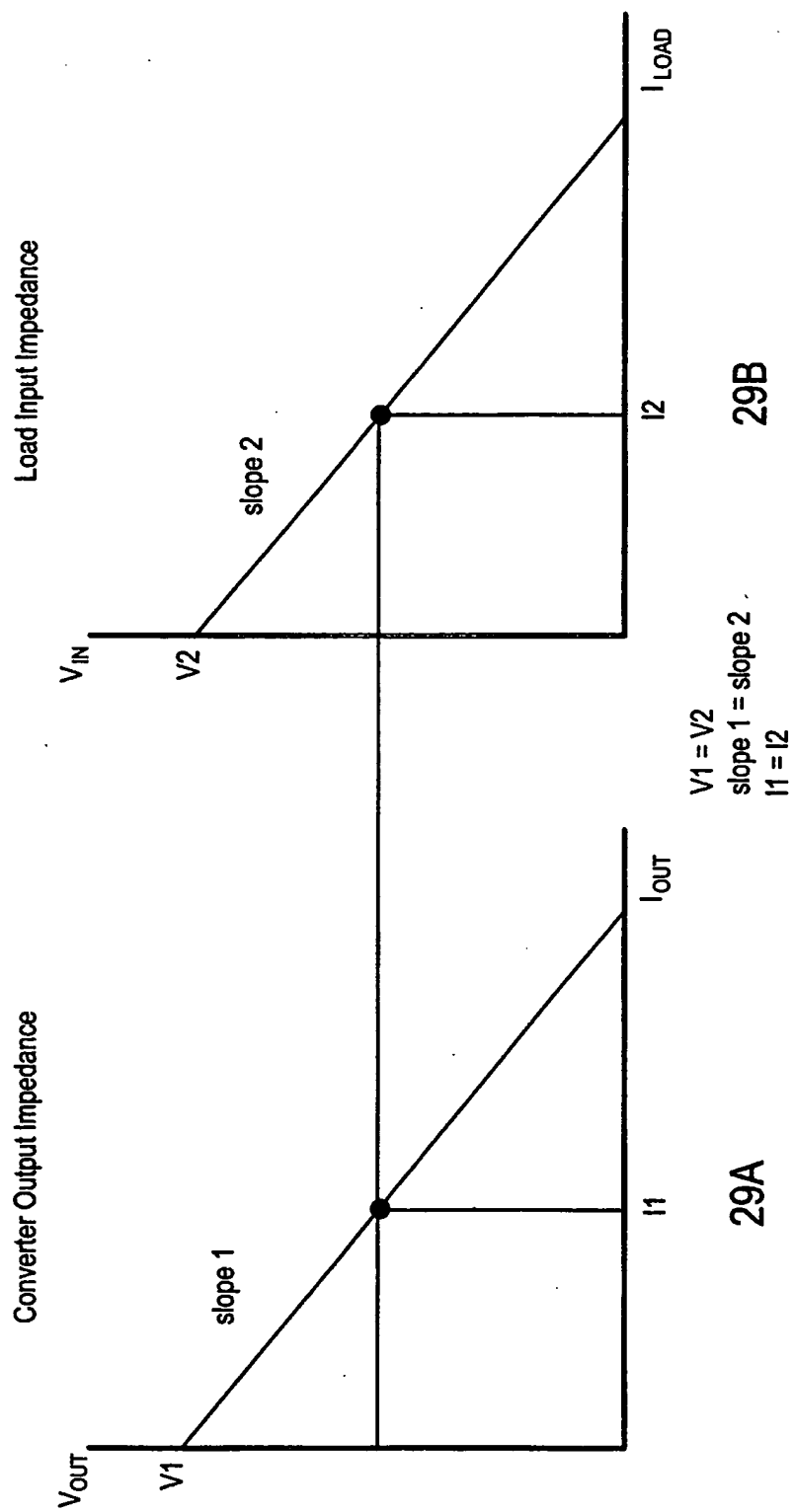


FIG. 29

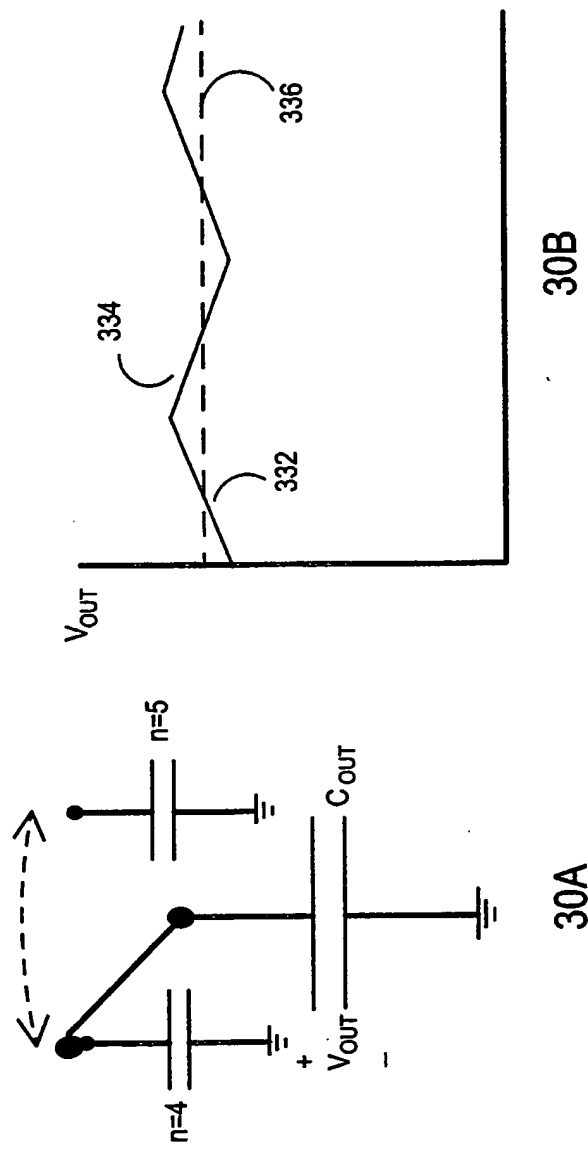


FIG. 30

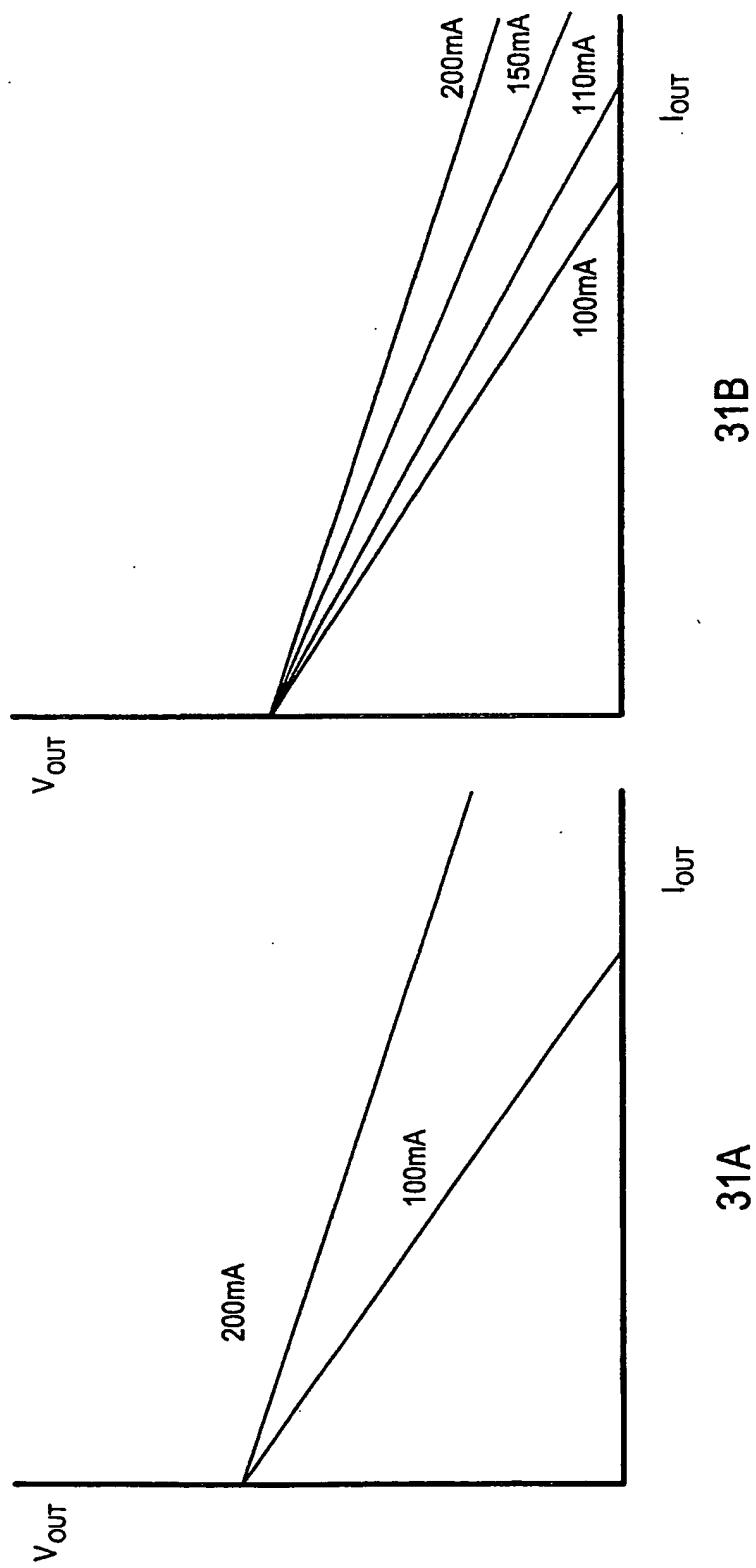


FIG. 31

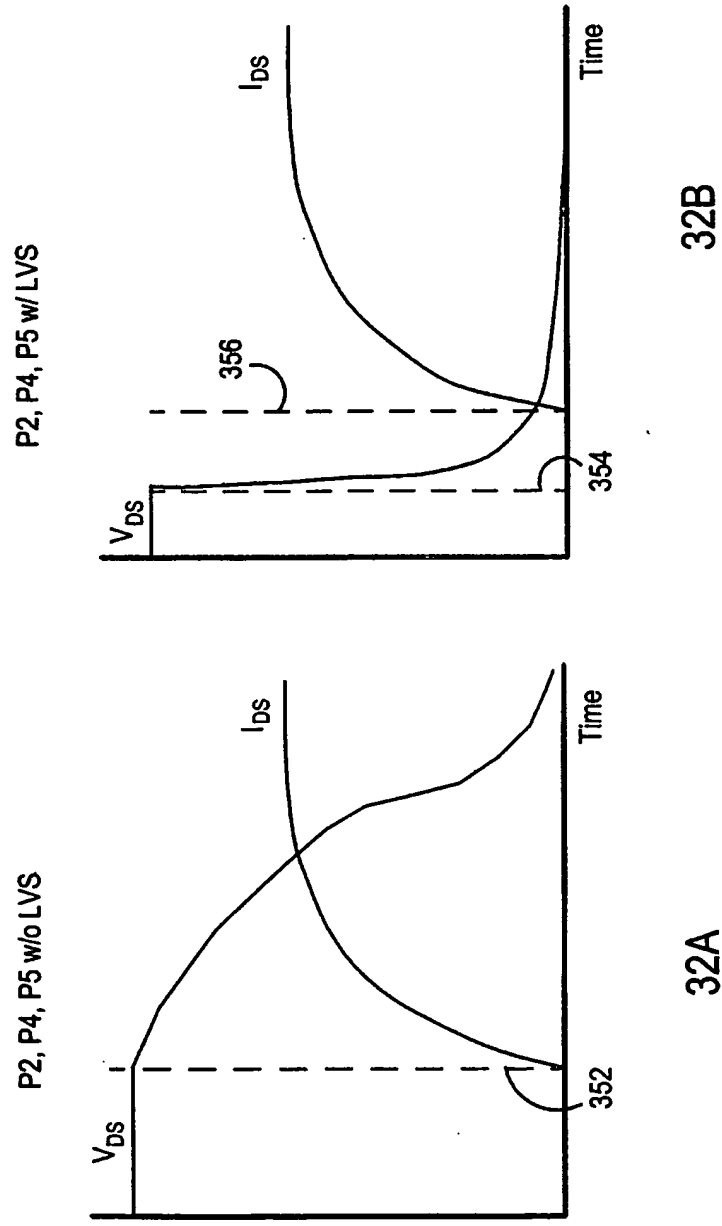
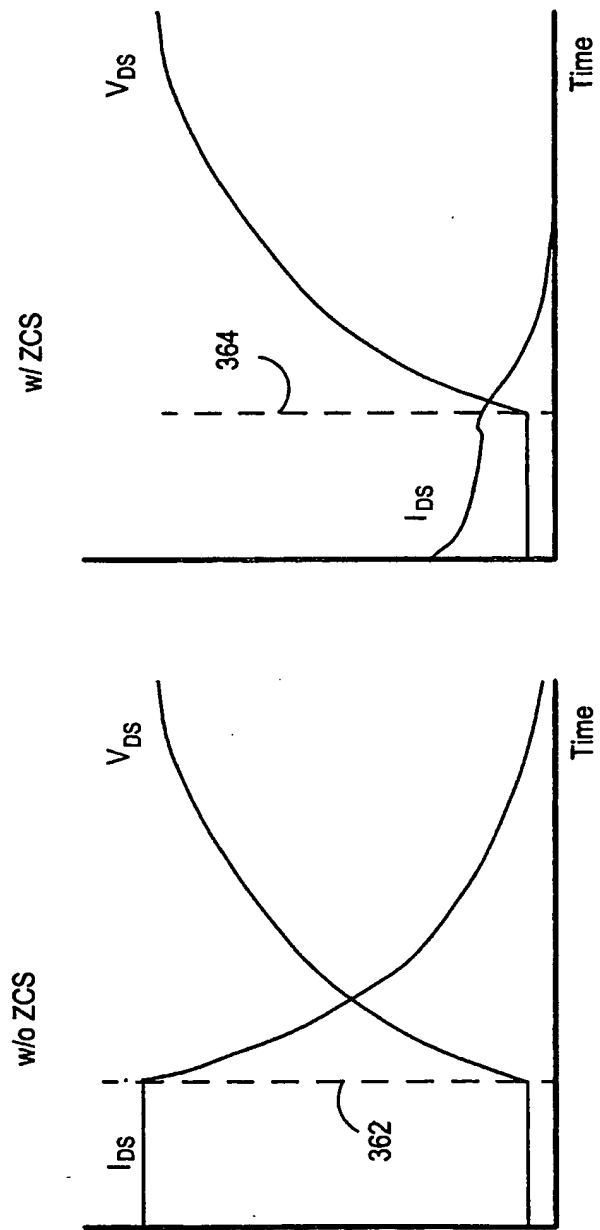


FIG. 32



33B

33A

FIG. 33

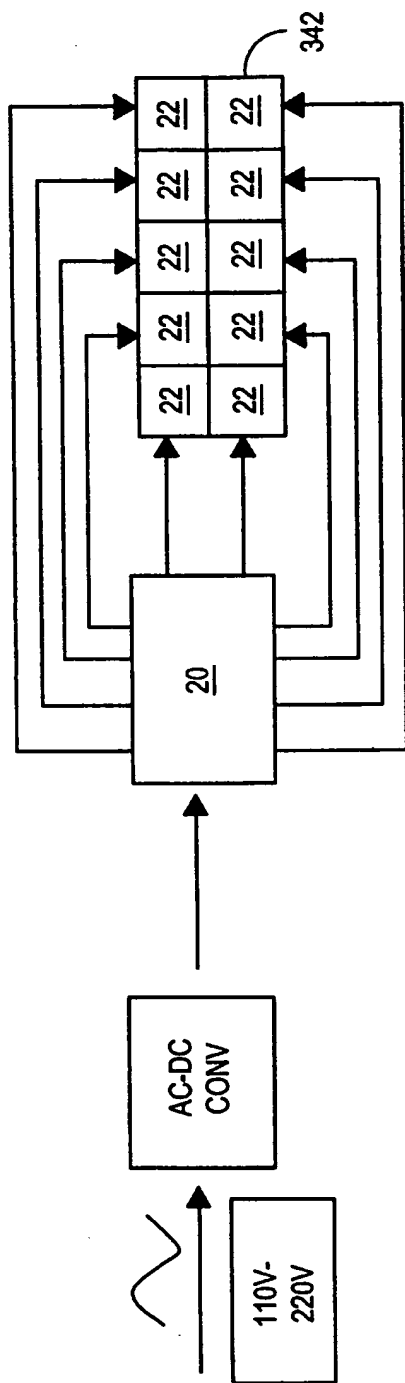


FIG. 34

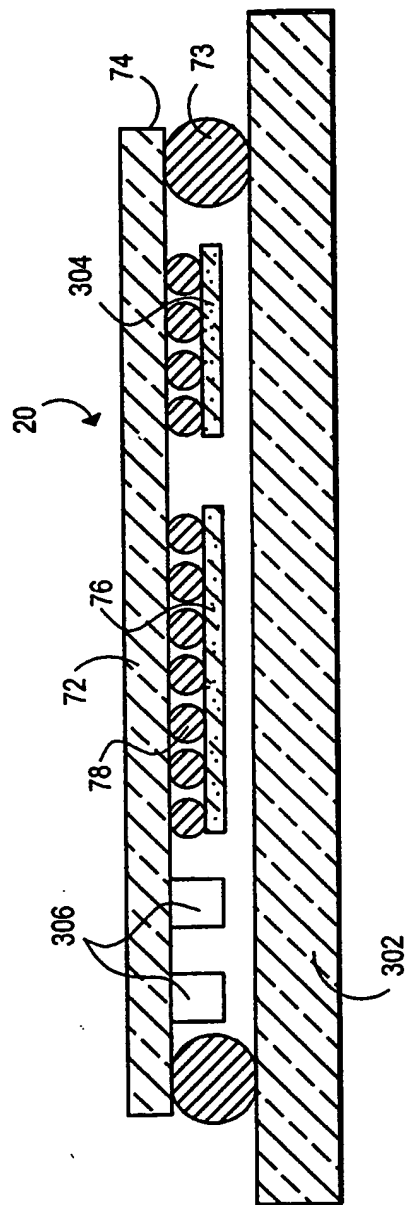


FIG. 35

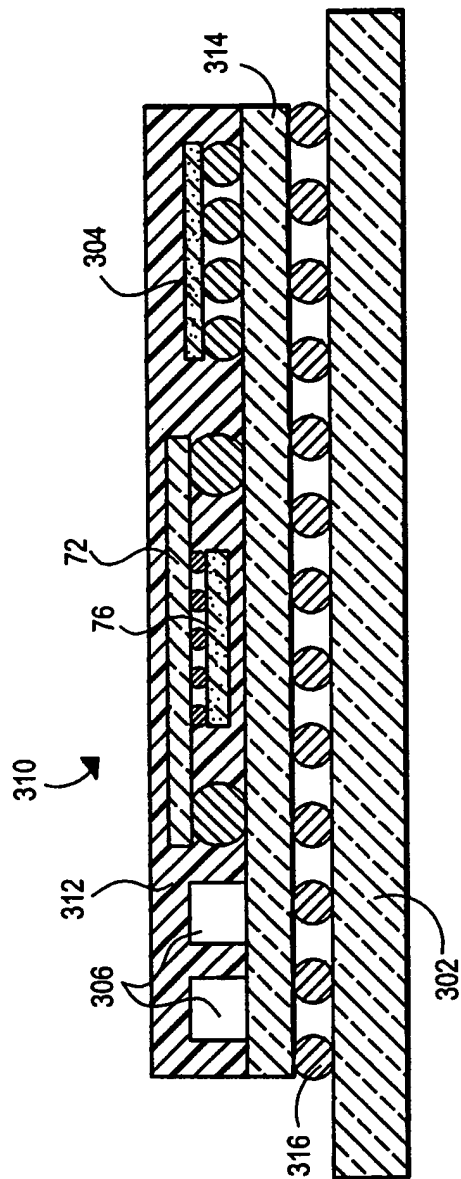


FIG. 36

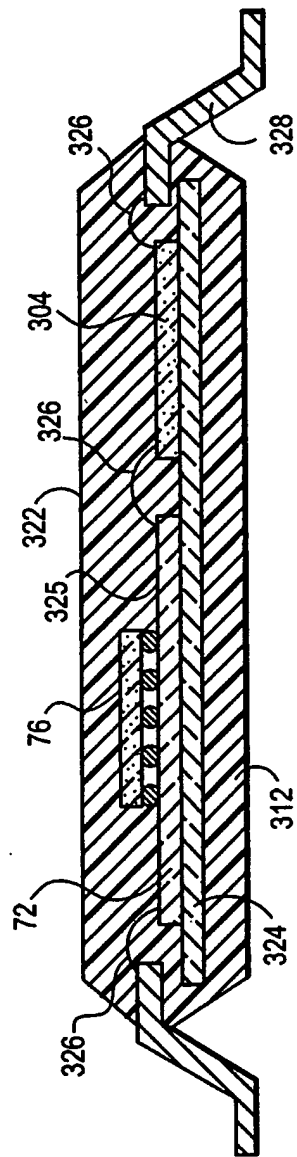


FIG. 37

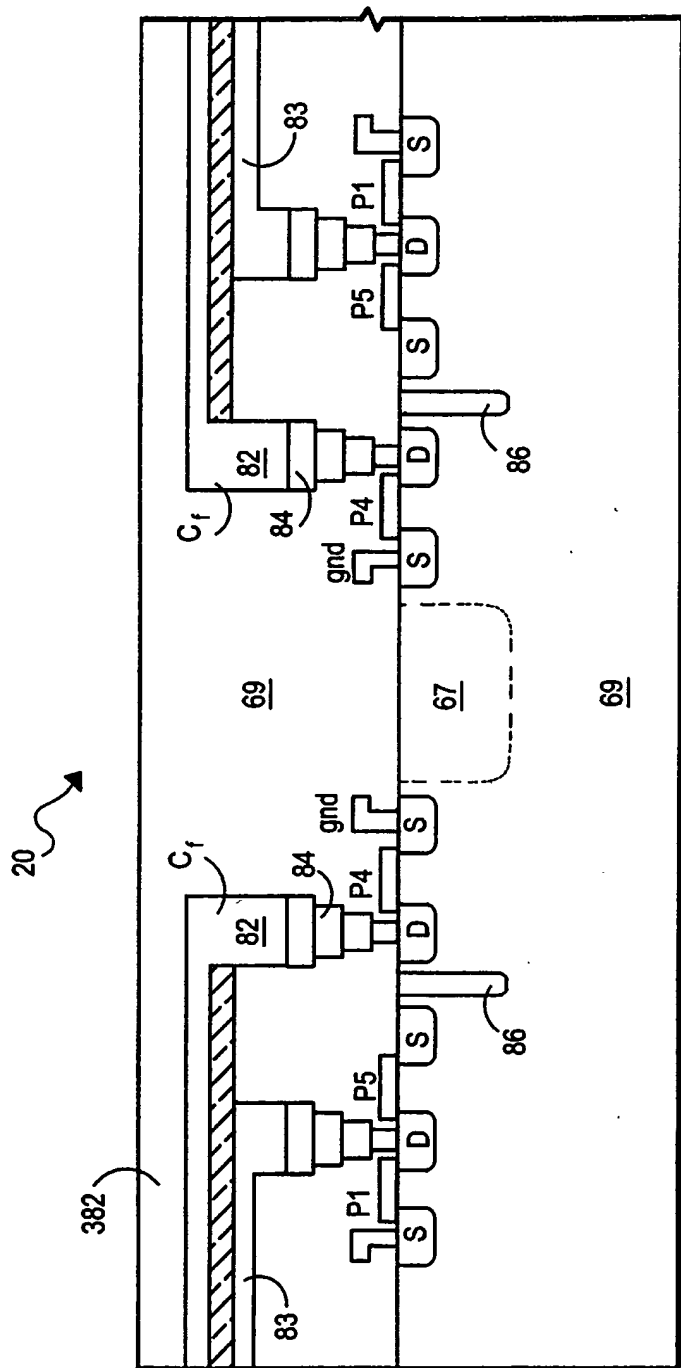


FIG. 38